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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number	10/734,294
Filing Date	December 15, 2003
First Named Inventor	Seon Yong CHA
Group Art Unit	2826
Examiner Name	Thomas L. Dickey
Attorney Docket Number	40296-0048

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

**Examiner
Signature**

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Considered

Not Considered

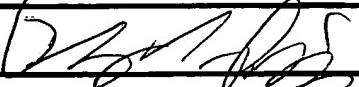
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/734,294
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				Examiner Name	Thomas L. Dickey
				Attorney Docket Number	40296-0048

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
	C09	XIANGDON CHEN et al., "Improved Hot-Carrier and Short-Channel Performance in Vertical nMOSFETs With Graded Channel Doping", IEEE Transactions on Electron Devices, 2002, p. 1962-1967, Vol. 49, No. 11		
	C10	W.J. GALLAGHER et al., "Microstructured magnetic tunnel junctions (invited)", J. Appl. Phys., 1997, pp. 3741-3746, Vol. 81, No. 8		
	C11	GITAE JEONG et al., "Magnetoresistance RAM with Self Reference Sensing. In: IEEE International Solid-State Circuits Conference, 9-13 Feb. 2003, S.1-8; "dual gate polysilicon", "Serially connected MTJ", A 0.24um 2.0V 1T1MTJ 16kb NV		
	C12	ABHINAV KRANTI et al., "Design Guidelines of Vertical Surrounding Gate (VSG) MOSFETs for Future UTSL Circuit Applications", IEEE, 2001, pp. 161-165		
	C13	K. McSTAY et al., "Vertical Pass Transistor Design for Sub-100nm DRAM Technologies", IEEE, Symposium On VLSI Technology Digests of Technical Papers, 2002, pp. 180-181		
	C14	Q. OUYANG et al., "Performance Enhancement in Vertical Sub-100NM NMOSFETs with Graded Doped Channels", IEEE, 2002, Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 17-19, 2002, pp. D016-1, D016-6		
	C15	WILLIAM REOHR et al., "Memories of Tomorrow", IEEE Circuits and Devices Magazine, September 2002, pp. 17-27		
	C16	G. SHRIVASTAV et al., "Performance Optimization of 60nm Channel Length Vertical MOSFETs Using Channel Engineering", IEEE, 2000, pp. 475-478		

Examiner Signature		Date Considered	Not Considered
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